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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,049	07/18/2001	Suresh Katukam	CISCP694	8487

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EXAMINER	
CHEA, PHILIP J	

ART UNIT	PAPER NUMBER
2153	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,049	KATUKAM ET AL.	
	Examiner	Art Unit	
	Philip J. Chea	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-11,19-27 and 37-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,19-27 and 37-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/22/02, 1/25/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed August 1, 2006. Claims 1-6,8-11,19-27,37-47 are currently pending, of which claim 47 is new. Any rejection not set forth below has been overcome by the current Amendment.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3,5,8-11,19,21-24,26-27,37-38,44-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Jain (US 2002/0112072).

As per claims 1, Jain discloses a system for computing paths between a first node and a second node within a network, as claimed, comprising:

- a memory (see paragraph [0063]);
- a route generator being arranged to generate a primary circuit path between the first node and the second node, the primary path including a first element selected from the plurality of elements (see paragraph [0079-0080], where primary path is a path from a base node to end node); wherein the route generator is arranged to accept an input, the input being arranged to specify one selected from the group including a nodal diverse constraint and a link diverse constraint for the alternate circuit path (see paragraph [0081] and [0098], where a node or link can be protected implying that an alternate node or link is implemented); and

- a list mechanism, the list mechanism being stored in the memory, the list being arranged to identify the first element, wherein the route generator is further arranged to generate an alternate circuit path between the first node and the second node using the list mechanism and the input, wherein the alternate circuit path does not include the first element identified by the list mechanism and a failure of the first element does not affect generating the alternate circuit path (see paragraph [0078 and [0081]).

As per claims 2, Jain discloses a system, as claimed, wherein the first element is a link (see paragraph [0098]).

As per claims 3, Jain discloses a system, as claimed, wherein the first element is a node (see paragraph [0098]).

As per claim 5, Jain discloses a system, as claimed, wherein the route generator is arranged to generate the primary circuit path that includes the first element and a set of elements (see paragraph [0098], where having a protected path implies that there is a primary path to protect), and the list mechanism is arranged to identify the first element and the set of elements as being inaccessible for use in generating the alternate circuit path (see paragraph [0098], where a protected path may be a series of links and nodes, implying a set of elements inaccessible for use in generating the alternate circuit).

As per claim 8, Jain discloses a system, as claimed, wherein when the input specifies the nodal diverse constraint, the first element is a node (see paragraph [0098]).

As per claim 9, Jain discloses a system, as claimed, wherein when the input specifies the link diverse constraint, the first element is a link (see paragraph [0098]).

As per claim 10, Jain discloses a system, as claimed, wherein the device is associated with the first node (see Jain paragraph [0063]).

As per claim 11, Jain discloses a system, as claimed, wherein the route generator is further arranged to implement the primary circuit and the alternate circuit path (see paragraph [0062]).

As per claims 19 and 24, Jain discloses an element for use in an optical network, the optical network including a plurality of links, the element comprising:

a memory (see paragraph [0063]);

a route generator, the route generator being arranged to compute a first circuit path between the element and the destination node, the first circuit path including a first link included in the plurality of links (see paragraph [0079-0080], where primary path is a path from a base node to end node) wherein the route generator is arranged to accept an input, the input being arranged to specify one selected from the group including a nodal diverse constraint and a link diverse constraint for a second circuit path between the element and the destination node (see paragraph [0098]), the input further being arranged to specify circuit characteristics for the first circuit path and for the second circuit path (see [0102]); and

a list, the list being stored in the memory, the list including a plurality of identifiers, the plurality of identifiers being arranged to identify selected links included in the plurality of links, the plurality of identifiers including a first identifier that identifies the first link, wherein the route generator is further arranged to compute the second circuit path using the list and the input, wherein the second circuit path includes a second link included in the plurality of links and does not include the selected links identified by the plurality of identifiers included in the list (see paragraph [0078-0081] and [0098]), wherein a failure of any of the selected links identified by the plurality of identifiers included in the list does not affect computing of the second circuit path.

As per claim 21, Jain further discloses a system, as claimed, wherein the element described in claim 19 is a source node (see paragraph [0077]).

As per claim 22, Jain further discloses a system, as claimed, wherein route generator identifies a first link to place in the list (see paragraph [0098]).

As per claim 23, Jain further discloses identifiers that are arranged to identify the selected links included in the plurality of links and to place the plurality of identifiers that are arranged to identify the selected links included in the plurality of links in the list (see paragraph [0080]).

As per claim 26, Jain further discloses an element applied to claim 23 above as a source node (see paragraph [0077]).

As per claim 27, Jain further discloses an element applied to claim 23 above to place the first identifier that identifies the first node in the list (see paragraph [0080]).

As per claim 37, Jain further discloses that the route generator is arranged to generate the primary circuit path and the alternate circuit path as nodal diverse paths in which the primary circuit path and the alternate circuit path have substantially no common nodes between the first node and the second node, and wherein when the primary circuit path and the alternate circuit path are the nodal diverse paths, the first element is a node (see paragraphs [0078-0081] and paragraph [0098]).

As per claim 38, Jain further discloses that the route generator is arranged to generate the primary circuit path and the alternate circuit path as link diverse circuit paths in which the primary circuit path and the alternate circuit path share substantially no links between the first node and the second node, and wherein when the primary circuit path and the alternate circuit path are the link diverse circuit paths, and the first element is a link (see paragraphs [0078-0081] and paragraph [0098]).

As per claim 44, Jain discloses a method for computing circuit paths between a first node and a second node within a network, the network including a plurality of elements, the network comprising:

receiving an input, the input being arranged to specify one selected from a group including a nodal diverse constraint and a link diverse constraint for an alternate circuit path between the first node and the second node relative to a primary circuit path between the first node and the second node, the input further being arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path (see paragraph [0098] and [0102]);

generating the primary circuit path, the primary circuit path including a first element selected from the plurality of elements, wherein generating the primary circuit path includes accounting for the specified circuit characteristics (see paragraph [0102-0103]);

creating a list, the list being arranged to identify the first element (see paragraph [0080]);

storing the list in a memory (see paragraph [0080] and [0063]); and

generating the alternate circuit path to not include the first element and to account for the specified circuit characteristics, wherein generating the alternate circuit path includes accessing the stored list and identifying the first element stored in the first list as being blocked from use in routing the

alternate circuit path and wherein a failure of the first element does not affect generating the alternate circuit path (see paragraph [0080-0081]).

As per claim 45, Jain further discloses that the specified circuit characteristics include one selected from a group including a shortest path characteristics and a load balancing characteristic (see paragraph [0084]).

As per claim 46, Jain further discloses that the nodal diverse constraint specifies that any nodes in the primary circuit path between the first node and the second node are not included in the alternate circuit path and wherein the link diverse constraint specifies that any links in the primary circuit path between the first node and the second node are not included in the alternate circuit path (see paragraph [0098] and [0081]).

As per claim 47, Jain further discloses that the circuit characteristics include a load characteristic (see paragraph [0103]).

- Claim Rejections - 35 USC § 103

3. Claims 4,6,20,25,39-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain as applied to claims 1, 5, 12,19,24 above, and further in view of Applicant's admitted Prior Art.

As per claims 4,6,20 and 25, Jain discloses means for identifying the link as being inaccessible to the alternate circuit path, wherein the means for including the identifier which identifies the first element as being inaccessible for use as a part of the alternate circuit path is arranged to include an identifier which identifies the link as being inaccessible to the alternate circuit path in the list (see paragraph [0078]).

Although the system disclosed by Jain shows substantial features of the claimed invention (discussed above), it fails to disclose the link being a protected link.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Jain, as evidenced by the Applicant.

In an analogous art, the Applicant discloses that it is old and well known in the art to have a network that contains protected links (see Specification page 2, lines 17-27). Further it would have been obvious to modify Jain by enabling the alternate circuit path to avoid the protected link and identify it as being inaccessible in order to avoid the high costs incurred of traversing the protected link.

As per claim 39, Jain in view of Applicants admitted Prior Art discloses a memory (see Jain paragraph [0063]);

a route generator being arranged to generate a primary circuit path between the first node and the second node, the primary path including a first element selected from the plurality of elements (see Jain paragraph [0080-0081]), wherein the route generator is arranged to accept an input, the input being arranged to specify one selected from the group including a nodal diverse constraint and a link diverse constraint for the alternate circuit path (see Jain paragraphs [0098]), the input further being arranged to specify a load characteristic that is to be accounted for when the alternate circuit path is generated (see Jain paragraph [0102-0103]); and

a list mechanism, the list mechanism being stored in the memory, the list being arranged to identify the first plurality of elements and at least one protected element (see Jain paragraph [0080] and discussion above regarding Applicants admitted Prior Art), wherein the route generator is further arranged to generate an alternate circuit path between the first node and the second node using the list mechanism and the input, wherein the alternate circuit path does not include the first plurality of elements and at least one protected element identified by the list mechanism (see Jain paragraphs [0078-0081], and discussion above regarding Applicants Prior Art).

As per claim 40, Jain in view of Applicants admitted Prior Art further discloses the first plurality of elements are link diverse constraint (see Jain paragraph [0098]).

As per claim 41, Jain in view of Applicants admitted Prior Art further discloses that the first plurality of elements are nodes if the input specifies a nodal diverse constraint (see Jain paragraph [0098]).

As per claim 42, Jain in view of Applicants admitted Prior Art further discloses that the list mechanism is a tabular list (see Jain paragraph [0063]).

As per claim 43, although Jain in view of Applicants admitted Prior Art does not expressly disclose that the tabular list includes a heading area that identifies the first plurality of elements and a heading area that identifies the at least one protected element, Jain does show that a table can be used to store possible points of failure that require protected links and/or nodes. At the time of the invention, a person skilled in the art would have found it obvious to include a heading area to identify the protected links and/or nodes and a heading area that identifies the at least one protected element in order to avoid the high costs incurred of traversing the protected link.

Response to Arguments

4. Applicant's arguments filed August 1, 2006 have been fully considered but they are not persuasive.

(A) Applicant contends that Jain does not show a list mechanism stored in memory that identifies an element.

(B) Applicant contends that Jain does not show an input being arranged to specify circuit characteristics.

(C) Applicant contends that Jain does not show an input that specifies a load characteristic that is to be accounted for when an alternate circuit path is generated.

In considering (A), the Examiner respectfully disagrees. Jain implies the claim limitation of a list mechanism stored in memory. The execution of the program described in Jain requires the use of computers that contain memory and implement data structures to store the elements along the calculated routes. The claim is not specific as to what type of list or how the list is implemented. Any set of data stored in memory can be considered a list as long as that set of data can be retrieved and sorted. The Examiner believes Jain is successful in producing a list to store the elements for a primary route and

diverse route. The Examiner invites the applicant to specifically claim the type of list, whether it be a linked list, array, tree, etc. in order to overcome the prior art rejection.

In considering (B), the Examiner respectfully disagrees. The claimed limitation of an input is broad enough to encompass a reasonable interpretation, which the Examiner believes Jain has evidenced. The input is unclear. The Examiner interprets the input to mean data to be entered into a computer for processing. The Examiner believes Jain teaches this reasonable interpretation. The Examiner invites the applicant to specifically claim how the input is introduced into the route generator, who/what provides the input, the format of the input, etc., in order to overcome the prior art rejection.

In considering (C), the Examiner respectfully disagrees. The Examiner has now cited paragraph [0103] showing a load characteristic that is accounted for when an alternate circuit path is generated.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip J. Chea whose telephone number is 571-272-3951. The examiner can normally be reached on M-F 7:00-4:30 (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Philip J Chea
Examiner
Art Unit 2153

PJC 10/4/06